



October 2, 2024

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Space 4

Space for a Safer World

Careers - Opportunities - Knowledge

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DELTA[△]TEC

LET'S DESIGN THE FUTURE



WHO IS DELTATEC?



BELGIAN

COMPANY

With international
activities



1986

DESIGN ACTIVITY

With strong focus on
embedded electronics

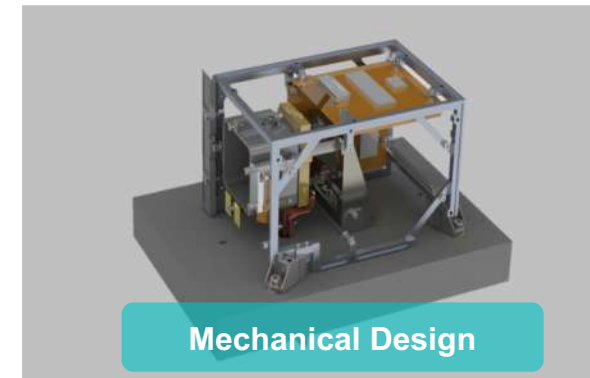
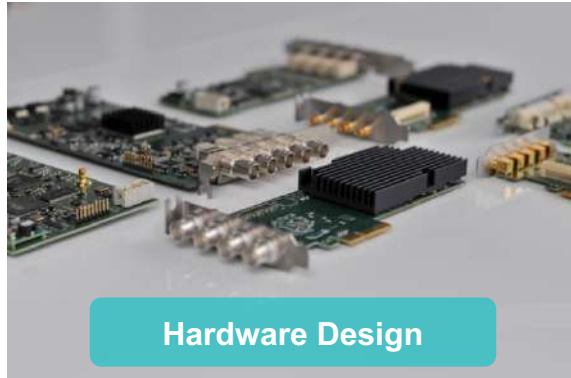


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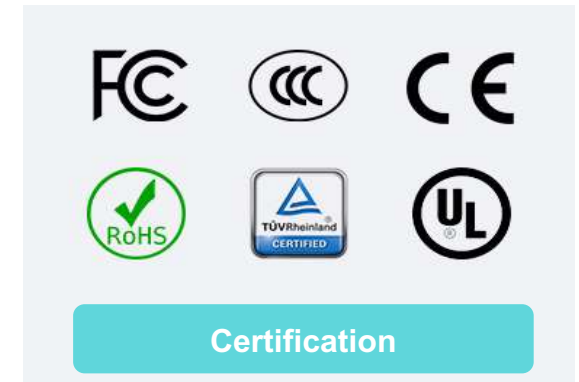
EMPLOYEES

Constantly growing

OUR SOLUTIONS



High-Tech ELECTRONIC and SOFTWARE design





5 ACTIVITIES AND BUSINESS UNITS

SERVICES

EMBEDDED



AEROSPACE



INDUSTRIAL
VISION



VIDEO
INTERFACE



AUGMENTED
REALITY



DELTACAST
VIDEO SOLUTIONS FOR DEVELOPERS

DELTACAST
VIRTUAL GRAPHICS FOR SPORTS

Based on a shared skilled engineering team

DELTATEC



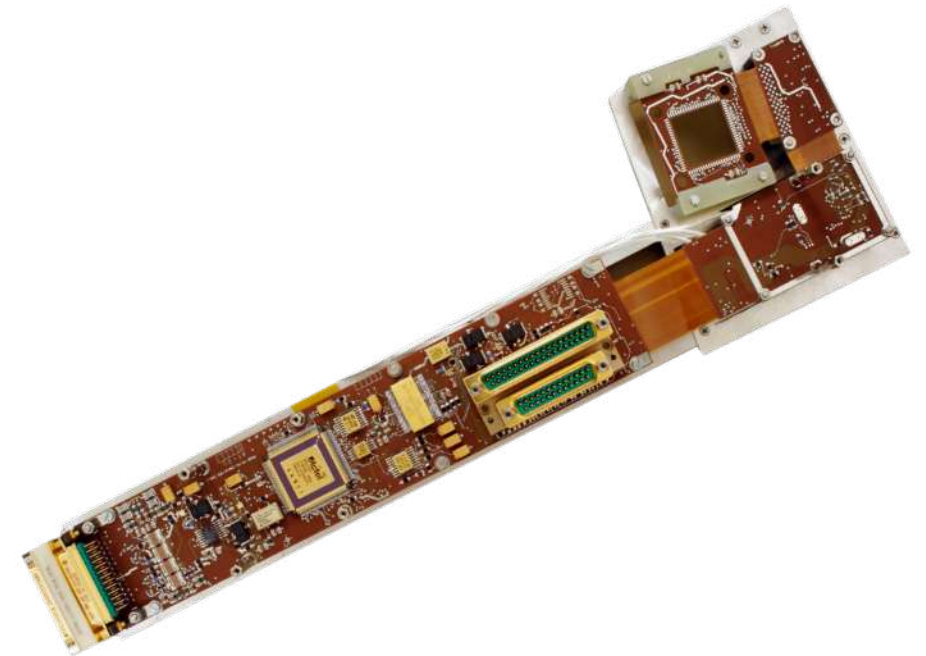
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Sun observation
using
CMOS Sensors



SWAP Instrument ROE

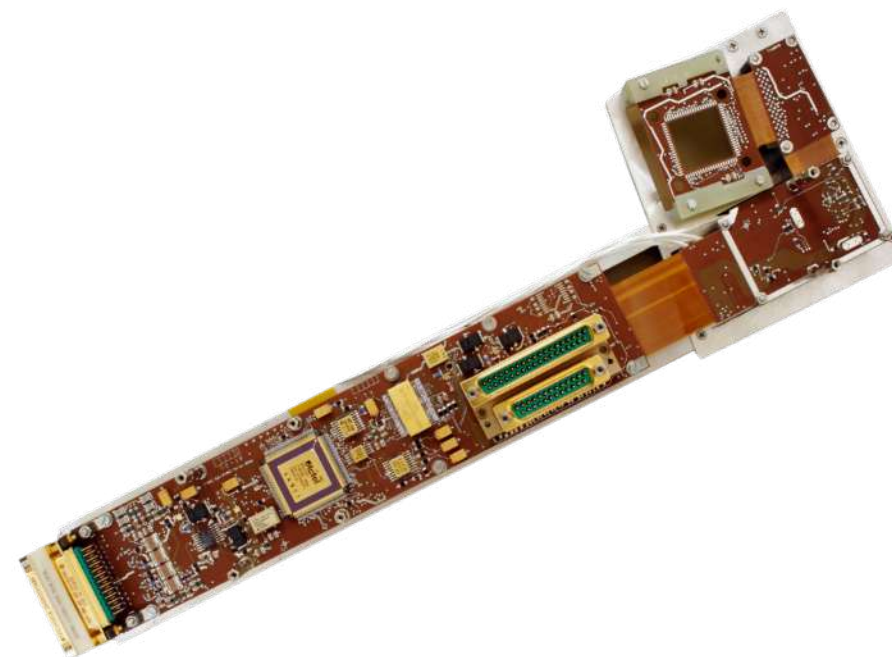
- In a nutshell
 - o First collaboration between CSL and DELTATEC Started in 2003





SWAP Instrument ROE

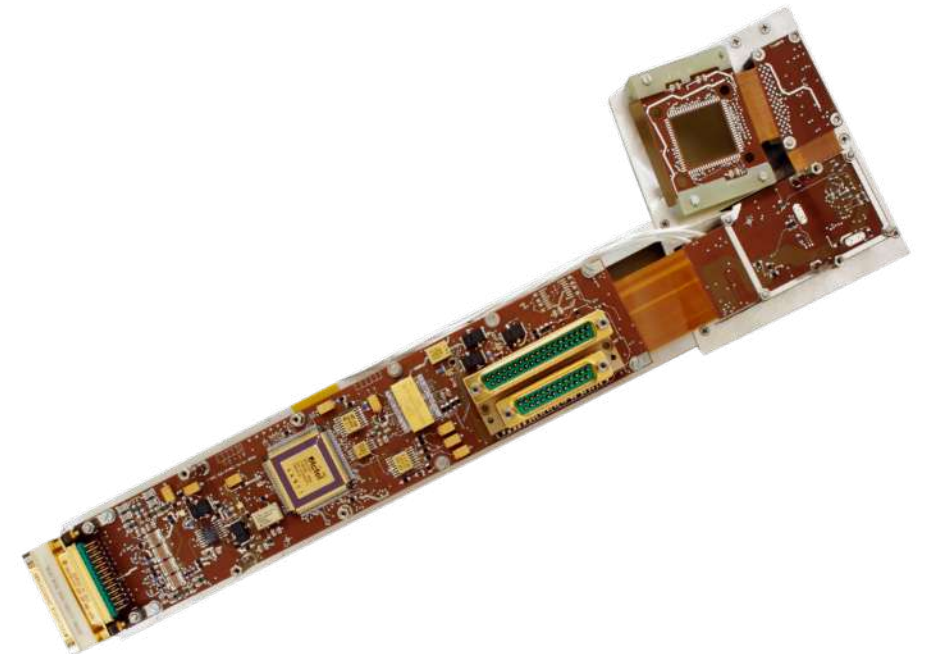
- In a nutshell
 - First collaboration between CSL and DELTATEC
 - First Space project for DELTATEC
 - ... but not the last !





SWAP Instrument ROE

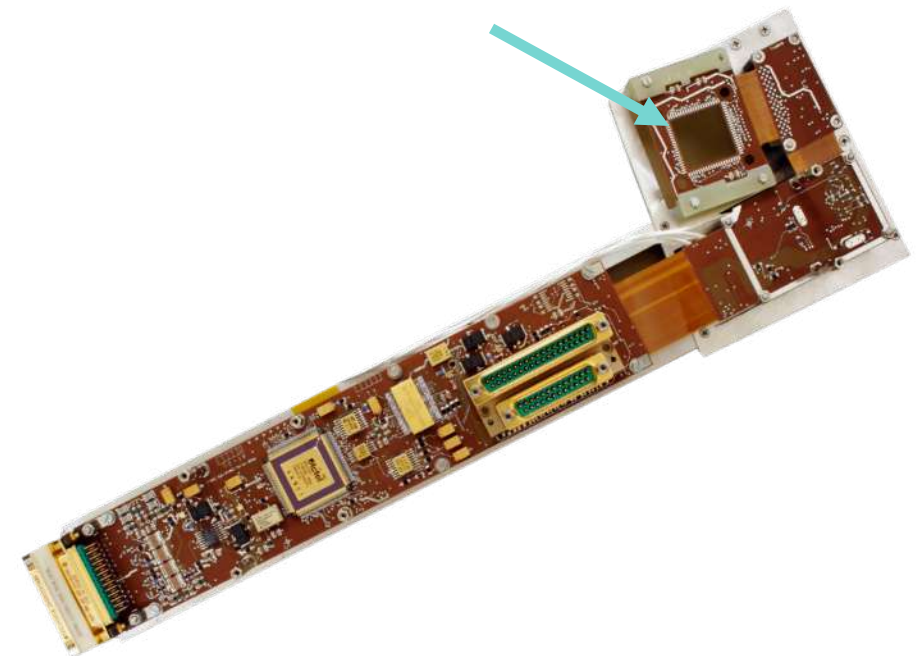
- In a nutshell
 - First collaboration between CSL and DELTATEC
 - First Space project for DELTATEC
 - Designed for a 2 years operation
... and still in operation 13 years later!





SWAP Instrument ROE

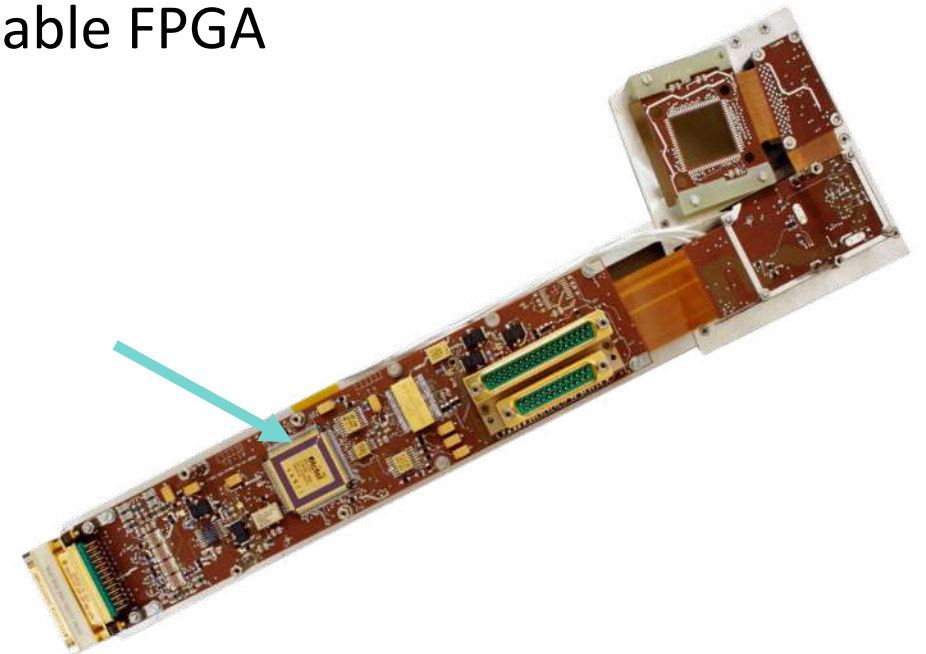
- In a nutshell
 - Based on HAS CMOS Sensor
 - ✓ High Accuracy Star tracker (HAS)
 - ✓ Radiation Tolerant
 - ✓ 1024 x 1024 pixels, 18um
 - ✓ 90-100 ke full well capacity
 - ✓ Designed in Belgium





SWAP Instrument ROE

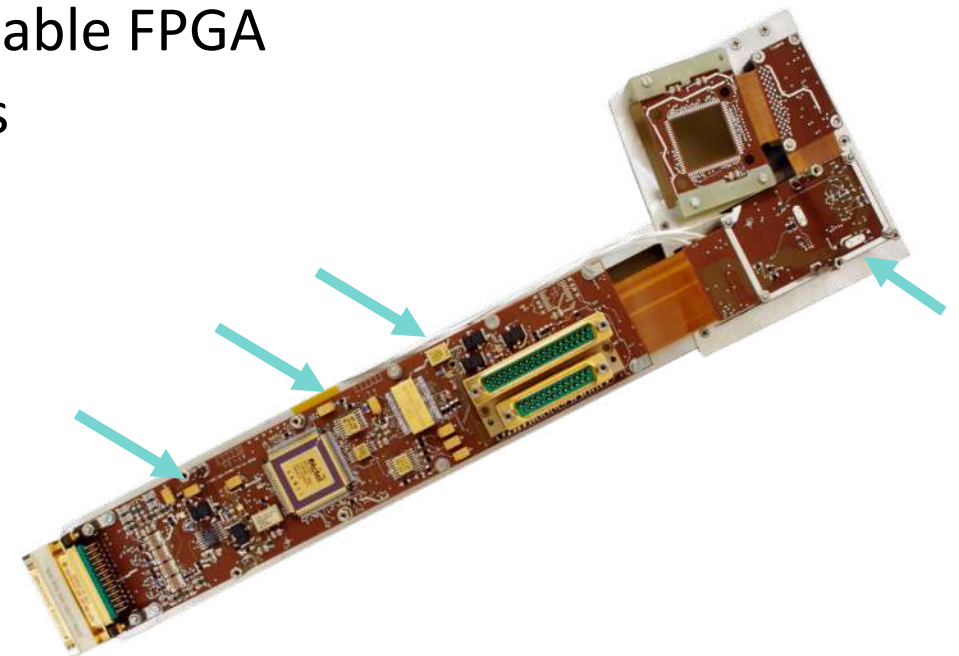
- In a nutshell
 - Based on HAS-2 CMOS Sensor
 - Sensor Control & Pixel extraction based on ACTEL/Microchip RTSX One Time Programmable FPGA





SWAP Instrument ROE

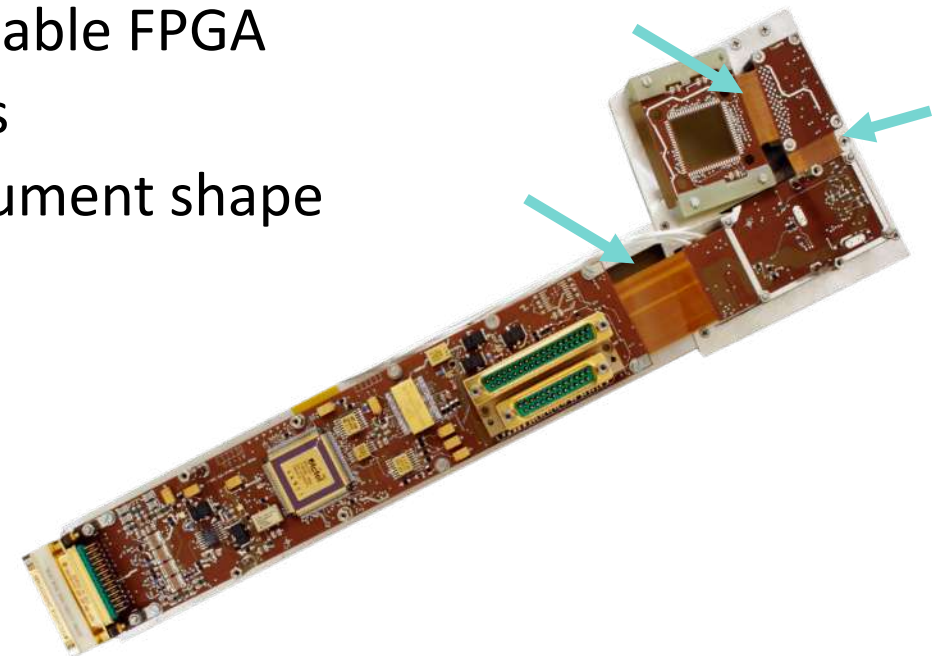
- In a nutshell
 - Based on HAS-2 CMOS Sensor
 - Sensor Control & Pixel extraction based on ACTEL/Microchip RTSX One Time Programmable FPGA
 - Rad-Hard / Rad-Tolerant EEE components





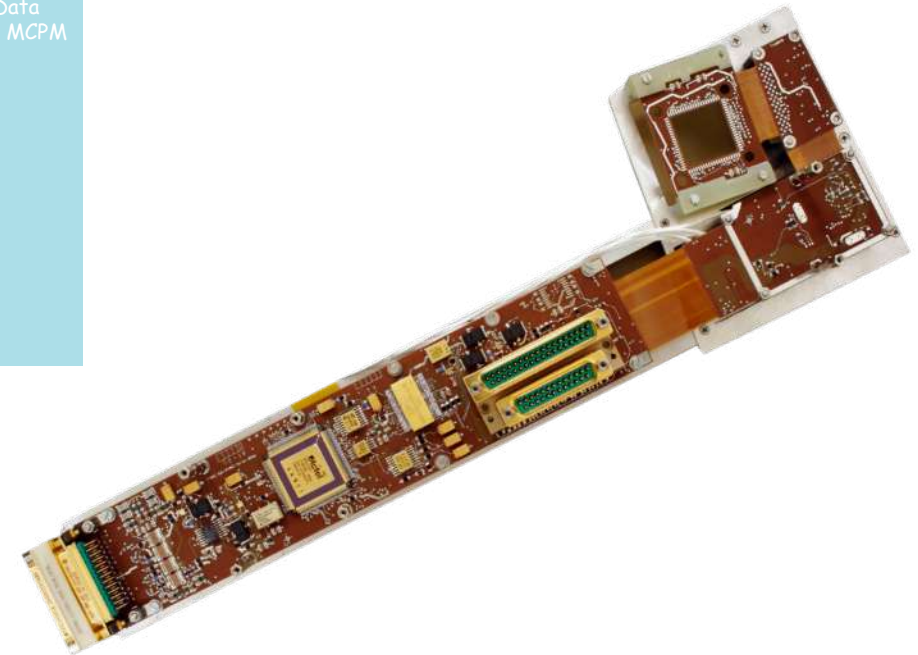
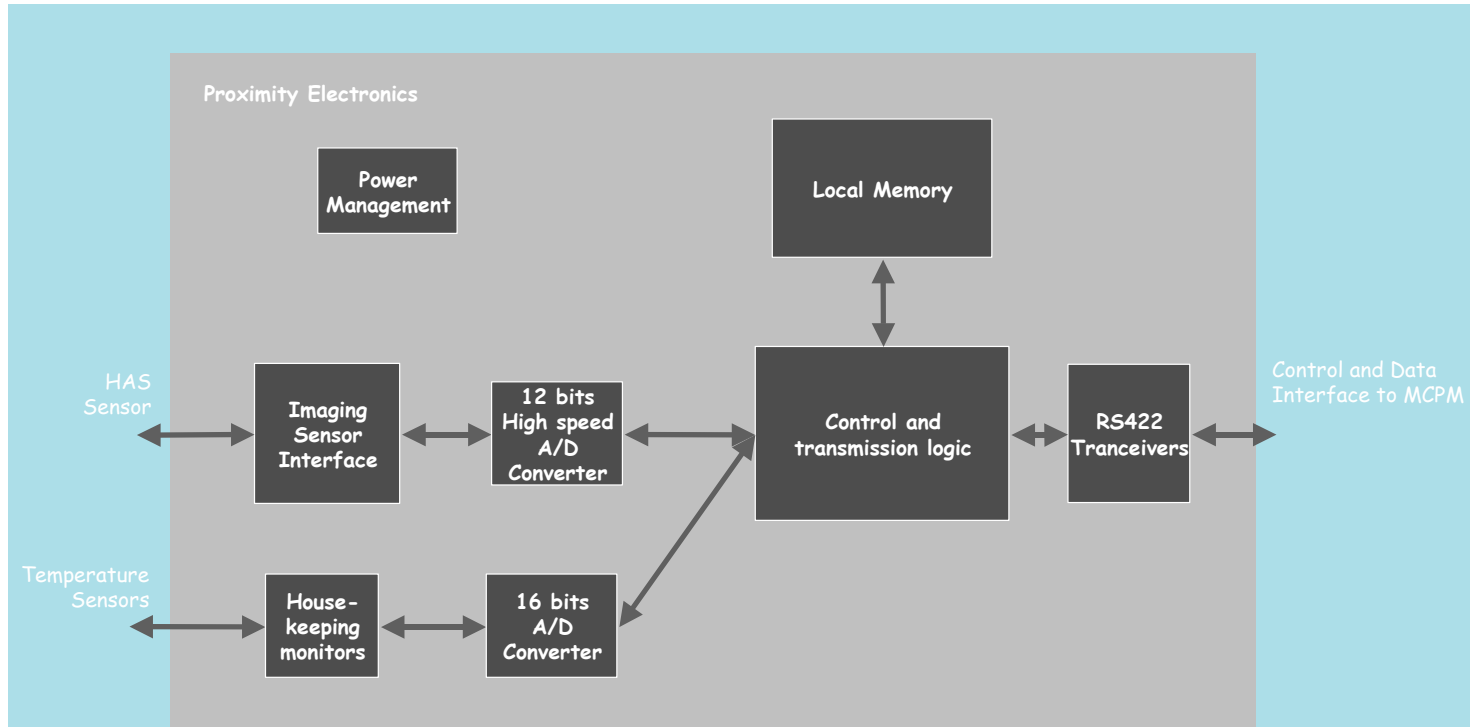
SWAP Instrument ROE

- In a nutshell
 - Based on HAS-2 CMOS Sensor
 - Sensor Control & Pixel extraction based on ACTEL/Microchip RTSX One Time Programmable FPGA
 - Rad-Hard / Rad-Tolerant EEE components
 - Flex-Rigid PCB to accommodate the instrument shape



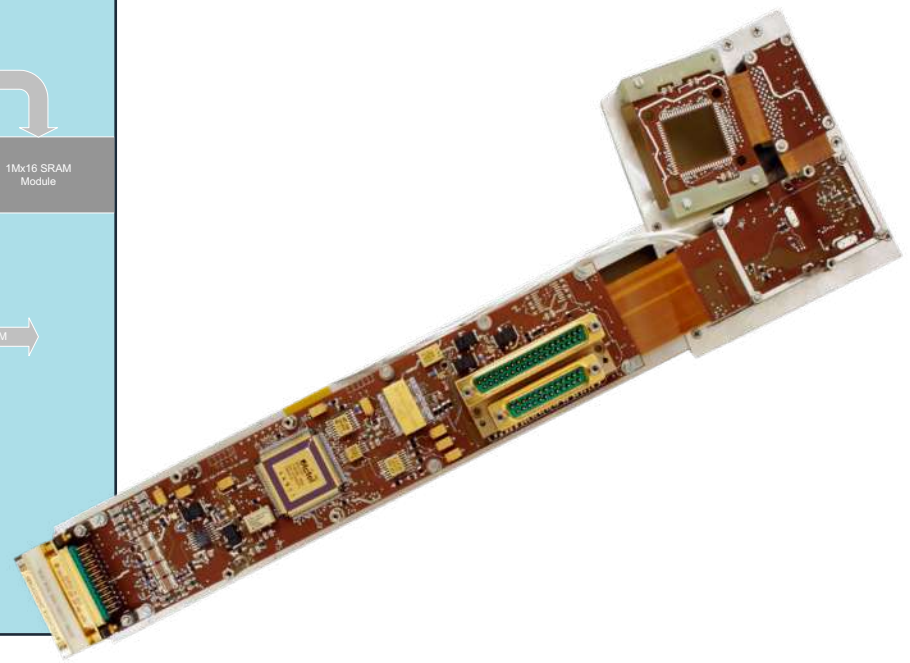
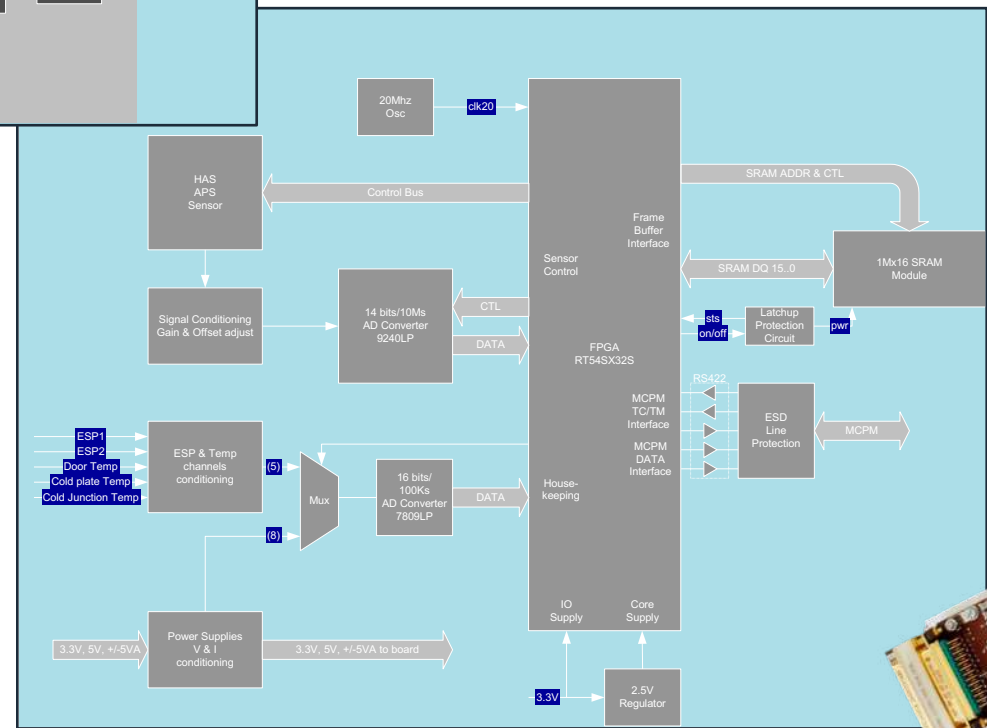
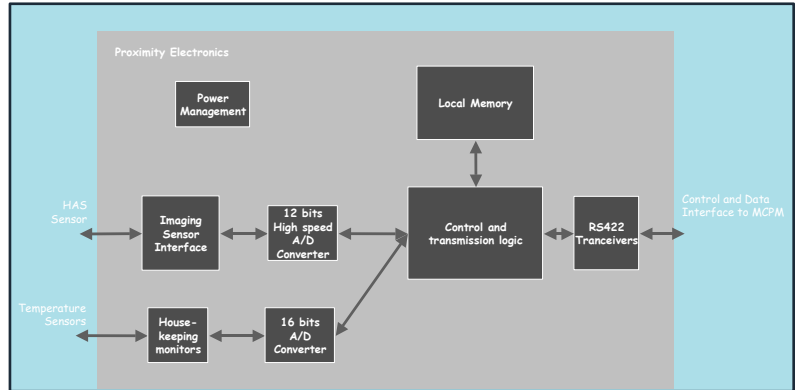


SWAP Instrument ROE





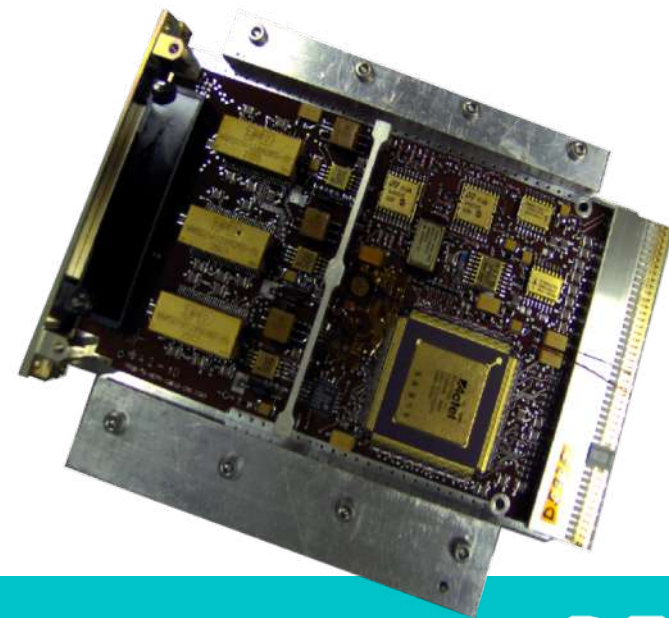
SWAP Instrument ROE





THE ROE ... and Our first MMU

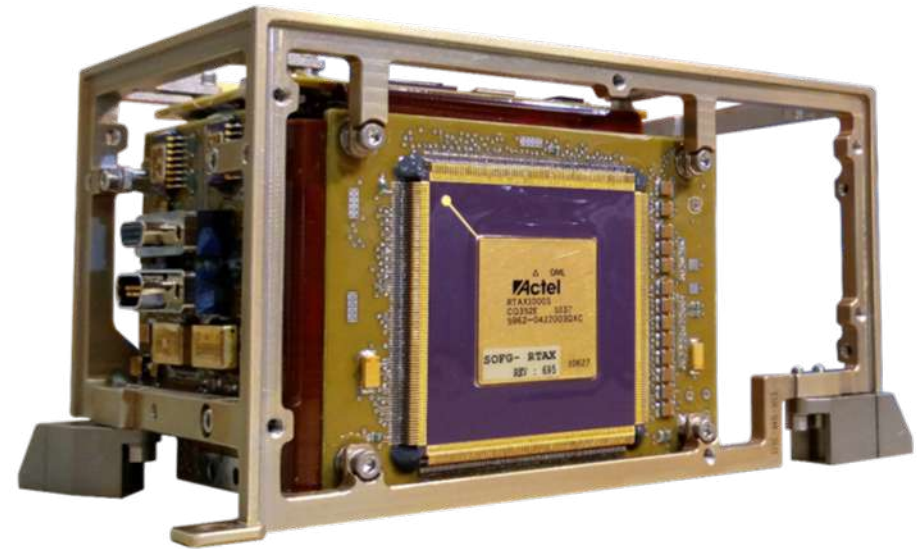
- COMPACT-PCI form factor (plugs in OBC)
- SDRAM technology
 - High density (4 Gb) ... we are in 2004 😊
 - Limited board space
 - High Bandwidth requirements
- Specific issues to tackle
 - Limited power
 - Radiation hardness
 - Error detection & correction (SEU)
 - Latchup/SEFI recovery
 - Thermal constraints





SOLAR ORBITER EUI Instrument ROE

- In a nutshell
 - o New collaboration between CSL and DELTATEC, Following SWAP successful experience.

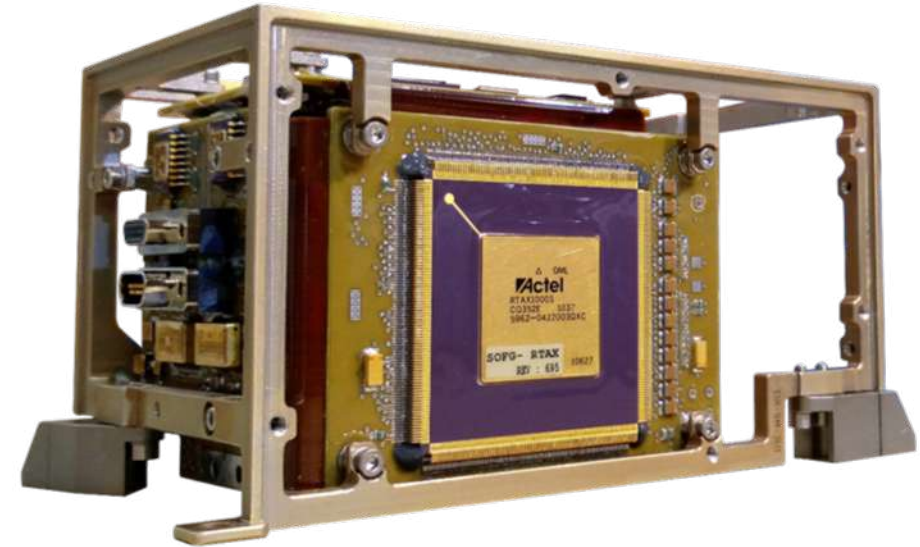




SOLAR ORBITER EUI Instrument ROE



- In a nutshell
 - Renewed collaboration between CSL and DELTATEC, Following SWAP successful experience.
 - Class 1 mission

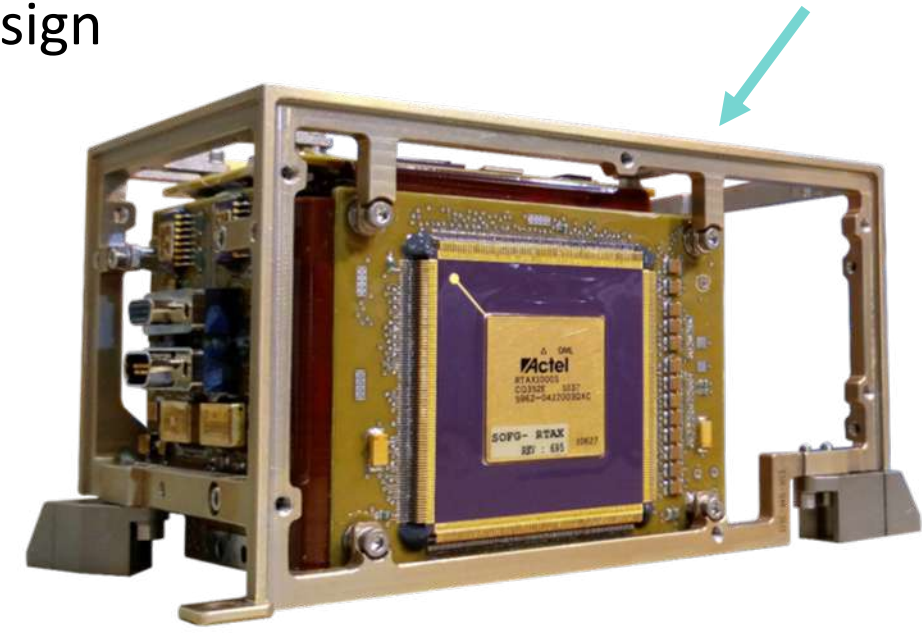
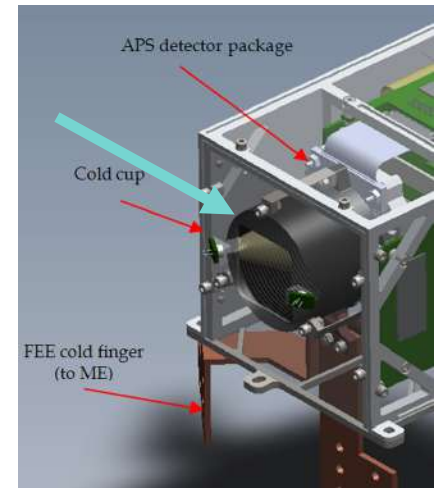
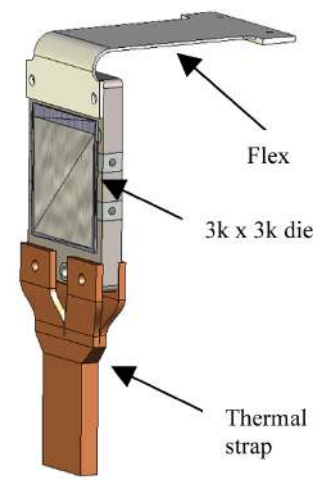
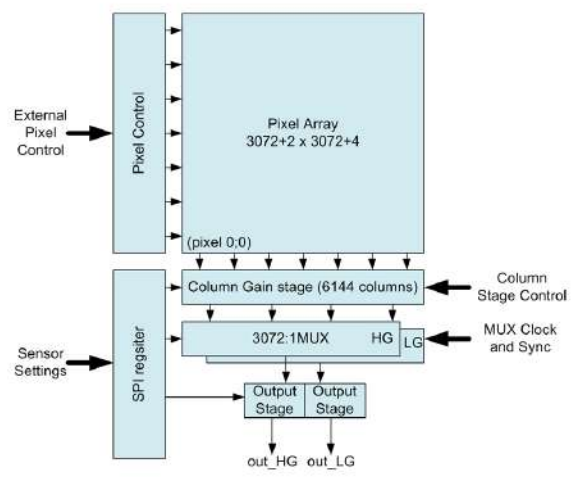




SOLAR ORBITER EUI Instrument ROE



- In a nutshell
 - o Mission specific APS CMOS sensors designed by CMOSIS/AMS (be)
 - ✓ dual-gain 10 μm back-thinned 3k x 3k
 - ✓ Not available at the time of the preliminary design
 - ✓ DELTATEC designed a sensor emulator

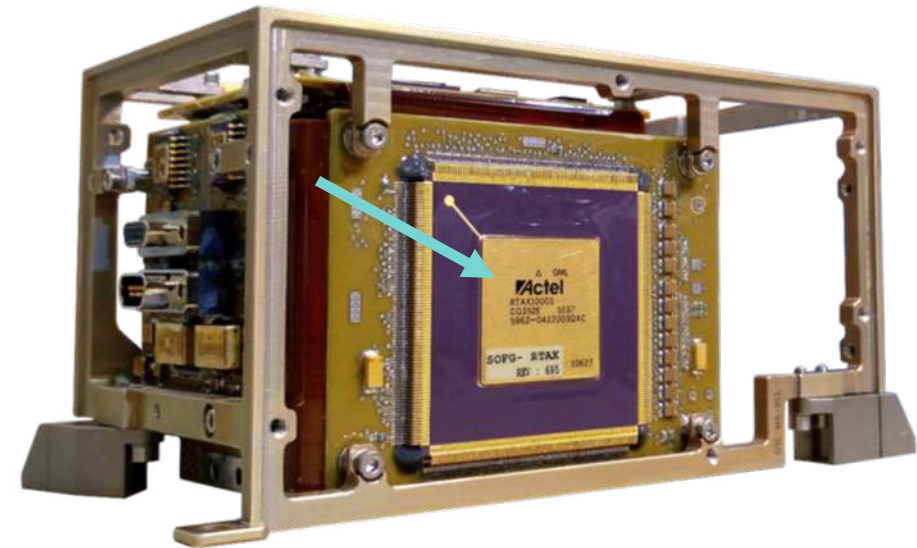




SOLAR ORBITER EUI Instrument ROE



- In a nutshell
 - Mission specific APS CMOS sensors designed by CMOSIS/AMS (be)
 - Sensor Control & Pixel extraction based on ACTEL/Microchip RTSX One Time programming FPGA
 - ✓ High-Reliability, Radiation-Tolerant, Antifuse





SOLAR ORBITER EUI Instrument ROE



- In a nutshell
 - Mission specific APS CMOS sensors designed by CMOSIS/AMS (be)
 - Sensor Control & Pixel extraction based on ACTEL/Microchip RTSX One Time programming FPGA
 - Class1 Mission Rad-Hard EEE components

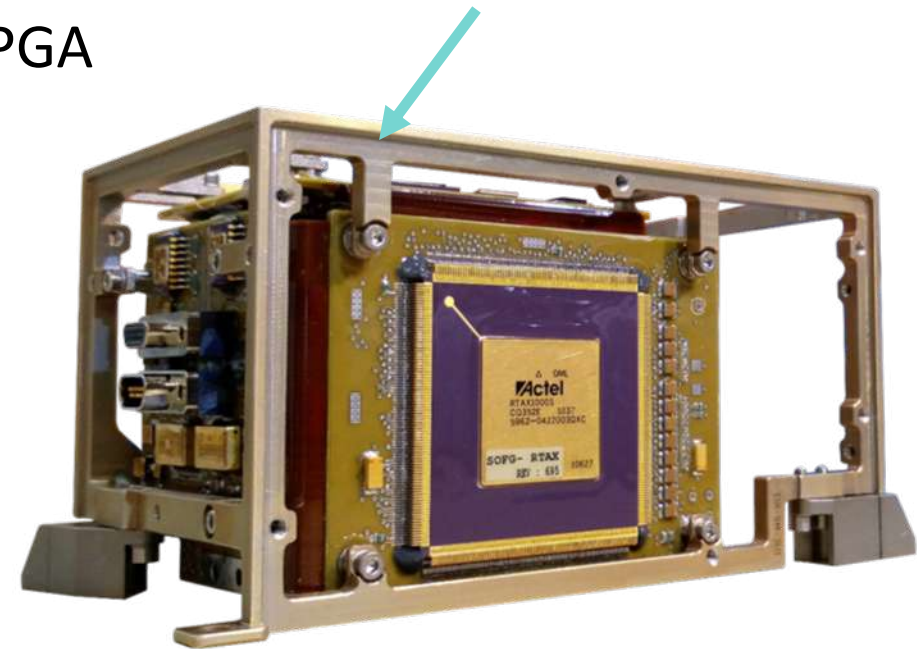




SOLAR ORBITER EUI Instrument ROE

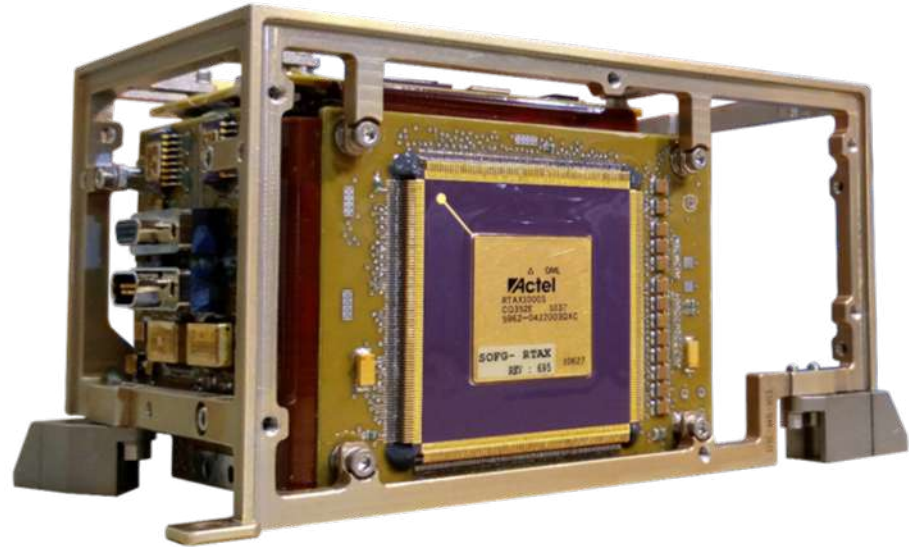
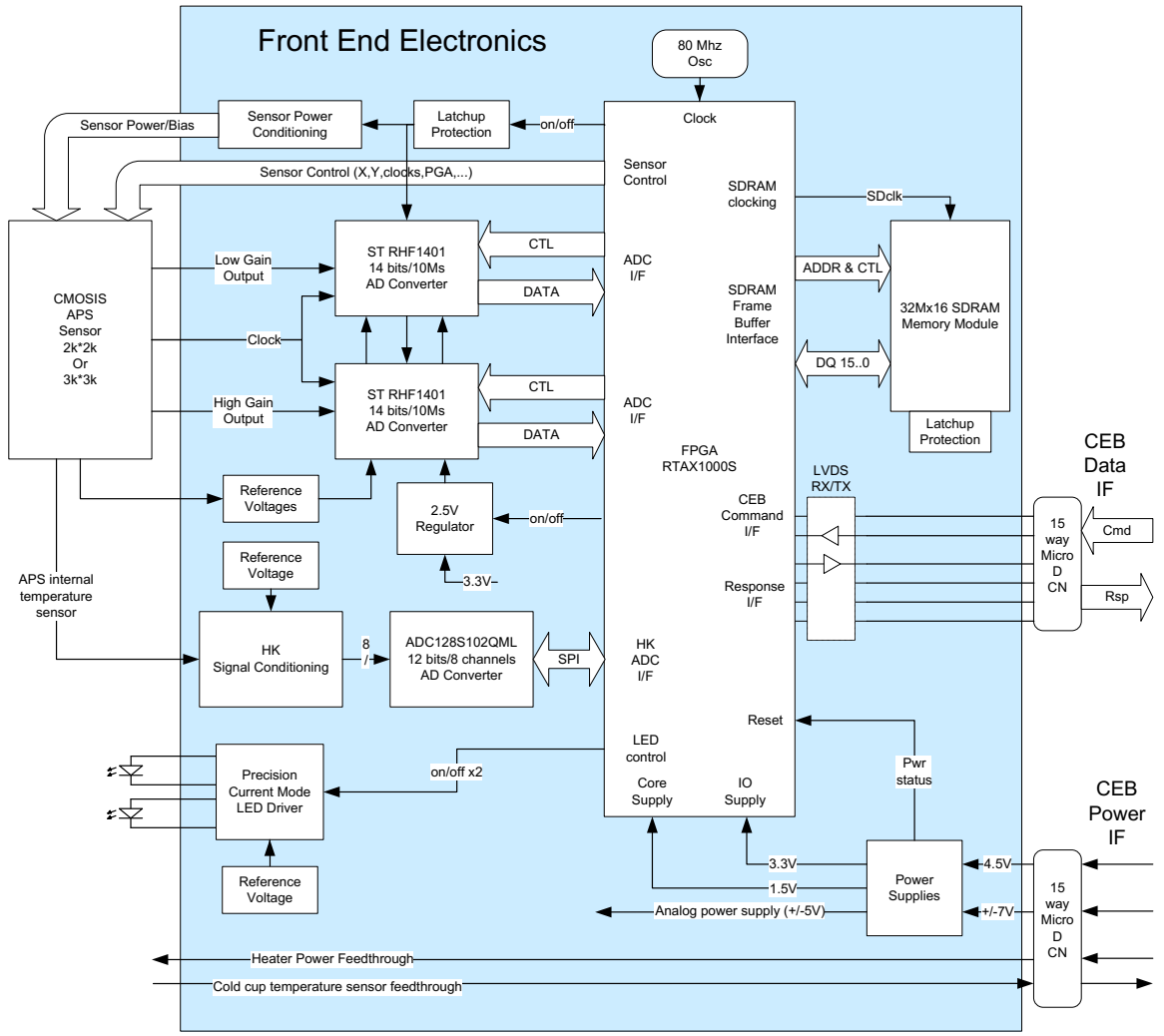


- In a nutshell
 - Mission specific APS CMOS sensors designed by CMOSIS/AMS (be)
 - Sensor Control & Pixel extraction based on ACTEL/Microchip RTSX One Time programming FPGA
 - Class1 Mission RadHard EEE components
 - Stringent Thermo-Mechanical constraints





SOLAR ORBITER EUI Instrument ROE





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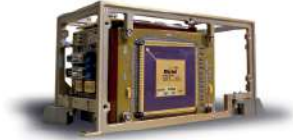
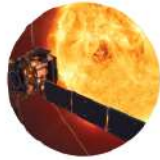
Space activities
The adventure continues

CAMERAS

EUI

Extreme UV Instrument on
SOLAR ORBITER mission

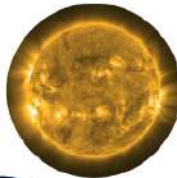
- ▶ Triple focal plane: mechanics & electronics
- ▶ Custom 9 MP CMOS detector from CMOSIS
- ▶ Stringent thermal / mechanical constraints
- ▶ TRL-9, launched in 2020



SWAP

EUV solar telescope (PROBA-2)

- ▶ Focal plane electronics
- ▶ HAS2 CMOS APS image sensor
- ▶ TRL-9, launched in 2009, designed for 2 years lifetime, still operating

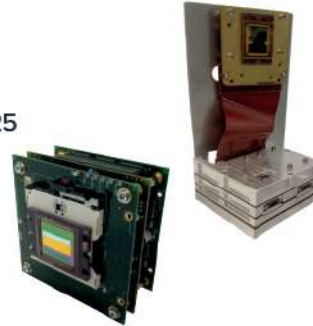


CSIMBA IOD

GSTP IOD Hyperspectral program



- ▶ Flexible and high speed sensor readout electronics
- ▶ 150 VIS spectral bands
- ▶ 1TB Mass Storage
- ▶ Gb ethernet interface
- ▶ TRL-7, launch target 2025



ELOIS ROES

GSTP IOD Hyperspectral program

- ▶ VNIR Electronics
- ▶ SWIR Electronics
- ▶ Payload Computer
- ▶ TRL-7, launch target 2025



THERMAL INFRARED (TIR)



For Earth Observation and in-orbit servicing

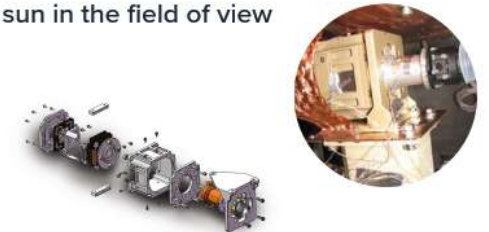
- ▶ NewSpace TIR Camera Core
- ▶ [8 - 14 μ m] SXGA 12 μ m pitch microbolometer
- ▶ Improved NETD and along track GSD
- ▶ CameraLink or LVDS interface
- ▶ 60Fps, 14 bits quantization
- ▶ TRL-4, ongoing RnD



CLS

Coarse Lateral Sensor for formation flying
missions (PROBA-3)

- ▶ Optical detector head mechanics & electronics
- ▶ Operates with sun in the field of view
- ▶ EM delivered
- ▶ TRL-6



DATA HANDLING AND PROCESSING

MMU

Mass Memory Units

SDRAM Based (512 Mb)

- ▶ Compact PCI I/F
- ▶ TRL-9, launched in 2009

Nand Flash Based (512/1024 Gb)

- ▶ SpaceWire I/F
- ▶ Leon3 + RTG4 architecture
- ▶ TRL-7, launch target 2025



AIS MISSIONS

Global ship traffic monitoring from space
(Satellite-based Automatic Identification
Systems of vessel)

- ▶ Dual redundant On-Board Computers
- ▶ Payload Computer including software
- ▶ TRL-9, launched in 2020



ELOIS PLC

GSTP IOD Hyperspectral program



- ▶ Dual payloads acquisition/processing/ recording system
- ▶ Hybrid architecture (Cost + Hardened Components)
- ▶ Integrates Radiation effects design mitigation technics
- ▶ Up to 6 LVDS I/F lines per payload at 100Mhz
- ▶ 1 TBytes of data Storage
- ▶ Cold redundant architecture
- ▶ TRL-5, launch target 2025



VESSELSAT 1&2

Microsatellite-based Automatic Identification
System of vessels (ORBCOMM)



- ▶ Low-power OBC (2W)
- ▶ COTS design, 160 Mhz RISC processor, extensive radiation mitigation
- ▶ TRL-9, launched in 2011 and 2012





Thank You

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